

REMARKS

Entry of this amendment is proper since no new claims or issues are raised and the only claim amendments are made to attempt to address the Examiner's newly-raised concerns with wording. Although Applicant brings to the Examiner's attention that claim wording does not have to be precisely the same as the original specification and Applicant believes that one having ordinary skill in the art would have found the rejected claim wording as completely supported in the original specification, Applicant has amended the independent claims to be consistent with the terms used in lines 1-9 of page 2 of the original specification. If this revised claim language is still unacceptable to the Examiner and since Applicant wishes to expedite prosecution, Applicant respectfully requests that the Examiner call Applicant's representative at the number below to discuss the Examiner's preferred wording.

Claims 1-16, 34, 35, and 38-39 are all of the claims pending in the present Application. Claims 17-33 and 36-37 are canceled and claims 38-39 have been added. Claim 9 is withdrawn from consideration until an allowable linking claim permits rejoinder.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-8, 10-16, 34, 35, 38, and 39 stand rejected under 35 USC §112, first paragraph, as allegedly failing to comply with the written description requirement.

Claims 1-8, 10-16, 34, and 35 stand rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, and 4-23 in the parent Application 09/759,101, now U.S. Patent 6,653,240, further in view of US Patent 6,010,918 to Marino.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, for example, in claim 1, the present invention is directed to a method for circuit modification of a microelectronic chip comprising at least one conductor

in an organic dielectric, in a manner so that a conductive residue from said ion-milling process does not contaminate said organic dielectric.

A protective inorganic surface layer is applied on the organic dielectric. A window is formed in the protective inorganic surface layer to selectively expose an underlying portion of the organic dielectric, the window being located over an area that covers a conductor to be modified by the ion-milling process. The organic dielectric is etched through the window to selectively remove a portion of the organic dielectric adjacent to the conductor.

The ion-milling process is performed on the conductor either to remove conductive material from the conductor to open up an existing routing in the circuit or to add conductive material to the conductor to form a new routing within the circuit.

As explained beginning at line 14 on page 1 of the specification, there is no conventional method that allows ion-milling to be used to modify circuits embedded in organic dielectric layer, since there is no known method that precludes the contamination of the organic dielectric layer during the ion-milling process. Without such method, as explained at lines 2-3 of page 2, ion-milling inherently utilizes charged ions that impregnate the organic dielectric to defeat electrical isolation.

In contrast, the present invention teaches that the organic dielectric layer be first selectively etched away from the conductor to be modified, so that the conductive residue from the ion-milling does not settle on the organic dielectric material adjacent to the operation. If necessary, the conductive residue from ion-milling process can specifically be also carried away by a passivation gas, such as xenon difluoride, introduced as part of the ion-milling procedure.

II. THE WRITTEN DESCRIPTION REJECTION

The Examiner again rejects claims 1-8, 10-16, 34, 35, 38, and 39 because the specification allegedly fails to describe that the conductive residue from the ion-milling does not contaminate the organic dielectric. In response, Applicant fails to see the Examiner's point, since the amended claim language would be well understood by one having ordinary skill and would indeed be considered as well supported by the description in the original

specification, particularly since claim language is not required to precisely match the wording of the specification.

However, in an effort to expedite prosecution, Applicant has changed the wording to use the terms used in lines 1-9 of page 2.

Applicant believes that the specification very clearly describes that the step of etching out the void space around the conductor eliminates or at least reduces the problem in the art of residual metal and ion impregnation of the surrounding organic dielectric layers, and the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE REJECTION BASED ON DOUBLE PATENTING

Claims 1-8, 10-16, 34, and 35 stand rejected under the judicially-created doctrine of obviousness-type double patenting over claims 1, 2, and 4-23 of the parent application, now US Patent 6, 653,240, further in view of US Patent 6,010,918. Applicant again respectfully traverses this rejection, and it is particularly noted that this rejection fails to address claims 38 and 39.

Therefore, Applicants submit that, without addressing all currently pending claims, this rejection becomes improper, since the terminal disclaimer would have to apply to all claims, including those not rejected.

However, Applicant respectfully submits that the Examiner's current rejection fails to establish a *prima facie* rejection for obviousness, since the method of newly-cited Marino is merely used to provide etching for emitter wells and is not used in a milling operation. Accordingly, there is no protection against contamination during ion milling being suggested in Marino.

It is noted that the Examiner's initial burden for establishing an obviousness rejection requires that the Examiner articulate a reasonable rationale to modify the primary reference in view of the primary reference itself. In the present evaluation, the Examiner is clearly and improperly using the claimed invention as roadmap, since Marino does not in any way suggest providing a gap around a conductor for purpose of reducing contamination, let alone contamination from an ion-milling processing. The only reasonable contribution that newly-

cited Marino brings to the evaluation is confirmation from another reference that etching of the claimed invention is possible, but such possibility by itself is not sufficient to establish a rationale for modifying the previously-allowed claims in the parent application to result in the claims of the present application.

As Applicant pointed out in his previous response, the Examiner clearly refused to allow claims of the parent application until Applicant incorporated into the independent claims the feature of exposing an underlying conductor. Therefore, the Examiner clearly considered the novelty of the claims of the parent application as necessitating this additional process of exposing the underlying conductor. The record remains unclear how the Examiner's double-patenting rejection is based upon considering that a void is formed around the upper conductor in these independent claims of the parent, since newly-cited Marino has nothing to do with ion-milling.

In contrast to the claims of the parent application, the independent claims of the continuation application do not require that a second underlying conductor be exposed and, instead, defines that contamination of the organic dielectric is avoided by removing portion of the organic dielectric to form a void space adjacent to the conductor. Removing this organic dielectric material means that there is no organic dielectric material adjacent to the conductor that will be contaminated during the subsequent milling.

These independent claims are clearly entirely different from the feature of the independent claims of the parent, wherein the Examiner required for allowability that there is defined an additional step of exposing an underlying conductor. To establish an obviousness rejection based on the claims of the parent application, the Examiner would have the initial burden of providing a reasonable prior art reference suggesting the void formed adjacent to the conductor, as described in the claims of the continuation that preclude contamination that would occur if this void were not present.

The Examiner fails to provide such prior art reference, let alone a reference to suggest recently-added dependent claims 37 and 38.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this double patenting rejection, particularly in view of the undue delay of the USPTO in taking up prosecution of the continuation application. Applicant respectfully

submits that such undue delay warrants the effect of a term adjustment, particularly in view that the prior art rejection relied upon for the parent rejection was never fully justified on the record.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-16, 34, 35, and 38-39, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance, since withdrawn claim 9 would be subject to rejoinder. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,



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